64. The structure of claim **53**, further comprising a slant field plate on the gate.

65. The structure if claim **53**, wherein the dielectric layer is between the cap layer and the gate.

66. The structure of claim **53**, wherein a layer of GaN laterally surrounds a gate region in which the gate is located.

67. An N-face enhancement mode high electrode mobility transistor device, comprising:

a substrate;

a heterostructure region and 2DEG region formed by a layer of AlGaN with a aluminum composition between 0 and 1 or equal to 1 and a GaN channel layer, wherein the heterostructure region is on the substrate and the GaN channel layer has a Ga-face adjacent to the layer of AlGaN; and

a cap in a recess of an N-face of the channel layer, wherein the cap does not overlie an access region of the device;

a gate formed on the cap; and

a source and drain on laterally opposing sides of the cap.

68. The device of claim **67**, wherein the cap is p-type Al_zGaN.

69. The device of claim **67**, wherein the cap comprises p-type Al_zGaN and AlN layers.

70. The device of claim **67**, wherein the cap includes Al_yGaN and Al_xGaN, and the Al_yGaN is closer to the gate than the Al_xGaN is and y>x.

71. The device of claim **70**, wherein the Al_yGaN and Al_x-GaN are doped p-type.

72. The device of claim **67**, wherein the cap includes Al_yGaN and Al_xGaN, the Al_yGaN is closer to the gate than the Al_xGaN is, Al_yGaN and Al_xGaN are doped p-type and x>y.

73. The device of claim **67**, wherein an access region between the gate and source and between the gate and drain is ion implanted.

74. The device of claim **67**, wherein an insulating layer is disposed between the gate and the cap.

75. The device of claim **67**, further comprising a dielectric passivation layer over at least the access region.

* * * * *